This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (currently amended) An electronic memory device comprising two or more layers of memory circuitry, each layer comprising circuitry for storing and ~~retrieving~~ facilitating retrieval of information and decoding circuitry for addressing specific information within said information storage circuitry, ~~and~~ wherein said two or more layers are interconnected by conductors ~~upon which are applied electrical signals that act as the control inputs~~at least some of which are also connected to said decoding circuitry ~~for addressing specific information~~.

2. (canceled) The memory device of claim 1 comprising conductors interconnecting the said two or more layers for carrying the information stored within the device.

3. (currently amended) The memory device of claim 1 wherein only a subset of the conductors ~~said applied electrical signals that act as the control inputs to said decoding circuitry for addressing specific information~~ are connected ~~applied~~ to the decoding circuitry ~~for addressing specific information of any given layer~~.

4. (currently amended) The memory device of claim 1 wherein each layer of memory circuitry comprises:

a first plurality of generally parallel ~~conductive means~~conductors;

a second plurality of generally parallel ~~conductive means~~ conductors overlapping and generally orthogonal to said first plurality;

~~a~~ non-linear conductive means interconnecting said first and second pluralities of conductors ~~generally parallel conductive means at~~ roughly ~~the points of~~ where they overlap;

decoding ~~means~~ circuitry for causing a first voltage on a selected one of the ~~conductive means of the~~ first plurality of conductors to differ from ~~the~~ voltages of the ~~remaining conductive means~~others of the first plurality of conductors; and

decoding ~~means~~ circuitry for causing a second voltage on a selected one of the second plurality of conductors ~~conductive means of the second plurality~~ to differ from the voltages of the others of the ~~remaining conductive means of the~~ second plurality of conductors,

wherein (i) ~~;~~

~~a voltage differential between said~~the first and second voltages differ sufficiently to forward bias a non-linear conductive means at any ~~said~~ point of overlap therebetween and (ii) ~~;~~

~~a~~ a voltage differential between ~~said voltages of~~ the non-selected ~~remaining conductive means~~ ones of the first plurality of conductors and ~~said voltages of the remaining conductive means~~ the non-selected ones of the second plurality of conductors ~~that~~ is ~~not~~ insufficient to forward bias a non-linear conductive means at any ~~said~~ point of overlap therebetween.

5. (original) The memory device of claim 4 wherein said non-linear conductive means are absent at some points of overlap.

6. (withdrawn) An electronic array circuit comprising:

a plurality of generally parallel rows and a plurality of generally parallel columns that are generally orthogonal and overlapping;

test circuitry comprising connections between the alternate ends of every evenly numbered row such that continuity of half of the rows can be tested by passing a current;

test circuitry further comprising connections between the alternate ends of every oddly numbered row such that continuity of the other half of the rows can be tested by passing a current.

7. (withdrawn) The array circuit of claim 6 comprising:

test circuitry comprising connections between the alternate ends of every evenly numbered column such that continuity of half of the columns can be tested by passing a current;

test circuitry further comprising connections between the alternate ends of every oddly numbered column such that continuity of the other half of the columns can be tested by passing a current.

8. (withdrawn) The array circuit of claim 6 comprising testing means for detecting a short-circuit between the evenly numbered rows and the oddly numbered rows.

9. (withdrawn) The array circuit of claim 7 comprising testing means for detecting a short-circuit between the evenly numbered columns and the oddly numbered columns.

10. (withdrawn) The array circuit of claim 7 comprising testing means for detecting a short-circuit between the rows and the columns.

11. (withdrawn) The array circuit of claim 6 wherein each row exists on a different layer of a multilayered, three-dimensional array.